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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/803,178	03/17/2004	Yasunori Kurosawa	81754.0114	4143

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EXAMINER	
DOAN, THERESA T	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 10/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

ER

Office Action Summary	Application No.	Applicant(s)	
	10/803,178	KUROSAWA ET AL.	
	Examiner	Art Unit	
	Theresa T. Doan	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *15-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 4-9 and 12-14* is/are rejected.

7)☒ Claim(s) *2,3,10 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/17/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-14 in the reply filed on 07/25/05 is acknowledged.

Drawings

2. The drawings, filed on 03/17/04, are accepted.

Information Disclosure Statement

3. The prior art documents submitted by applicant in the Information Disclosure Statement filed on 03/31/04, have all been considered and made of record (note the attached copy of form PTO-1449).

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

5. Claim 10 is objected to because of the following informalities:

In claim 10, line 2, a word "**with**" should be inserted before "a depth".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 4-6, 9 and 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hwang et al. (U.S. Pat. 6,455,408) in view of Hsuan et al. (U.S. Pat. 6,166,444).

Regarding claims 1 and 9, Hwang (Figs. 15-17) discloses a semiconductor device or wafer 50 (column 3, lines 52-53), comprising:

a semiconductor substrate 52 (column 3, lines 55-56) provided with a plurality of integrated circuits (not shown, see column 3, lines 54-56) and pads 54; a semiconductor chip 90 of the semiconductor wafer 50 provided with an integrated circuit (not shown, see column 3, lines 54-56) and a pad 54 (Fig. 17); a wiring layer 64 that has a concave portion 68 (column 4, lines 60-65) and is electrically connected to the pad 54; an external terminal 80 that is joined to the concave portion 68 of the wiring layer 64 (see Figs. 16-17 Labeled by the examiner below and column 5, lines 61-63); and a polyimide or epoxy resin layer 74 (column 5, lines 30-38 and column 3, lines 66-67 through column 4, lines 1-2) provided with a through hole and disposed on the wiring layer 64, the through hole and the concave portion 68 residing at the same position (see Fig. 16 below and column 5, lines 28-30).

Hwang discloses a semiconductor chip 90 provided with the integrated circuit and a pad 54, but does not specifically disclose that the pad 54 is electrically connected to the integrated circuit.

However, Hsuan (Fig. 3) teaches a semiconductor chip 30 provided with an integrated circuit 32 and a pad 42 (column 3, lines 19-20), the pad 42 is electrically connected to the integrated circuit 32 (column 3, lines 15-17) and to the external terminals 56. Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to provide the semiconductor chip of Hwang with the pad 54 electrically connected to the integrated circuit in order to provide the electrically connects between the integrated circuit and the external terminals, as taught by Hsuan (see Fig. 3).

FIG. 16

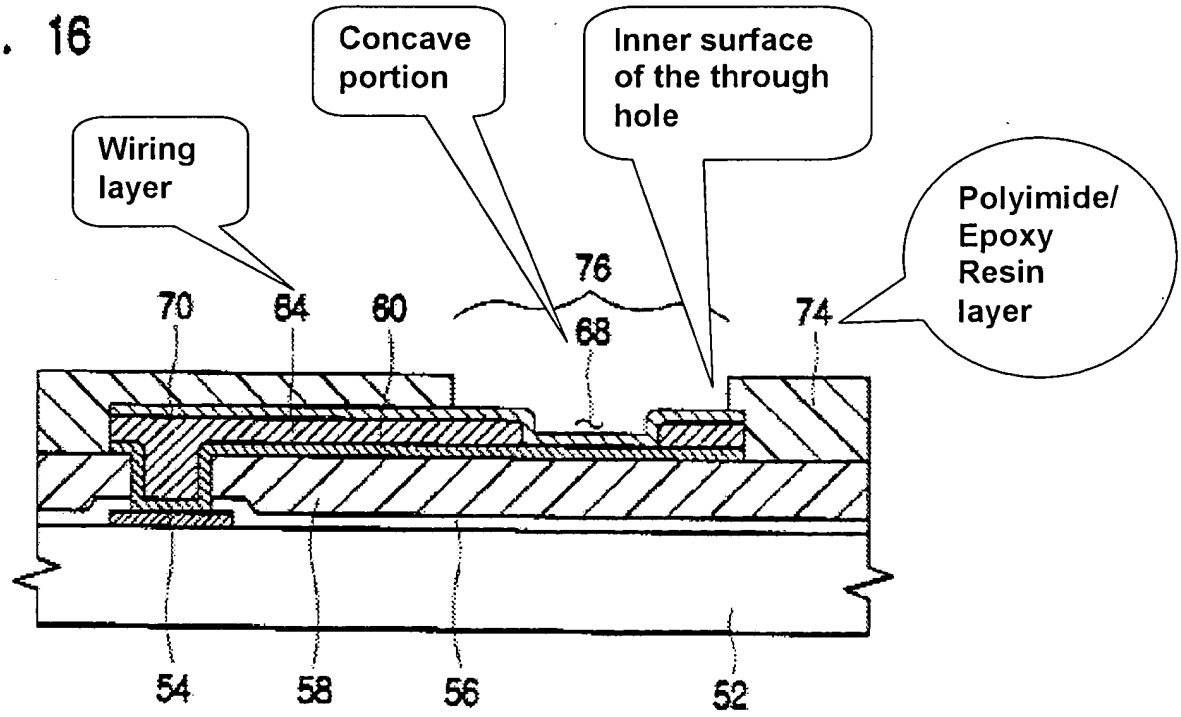
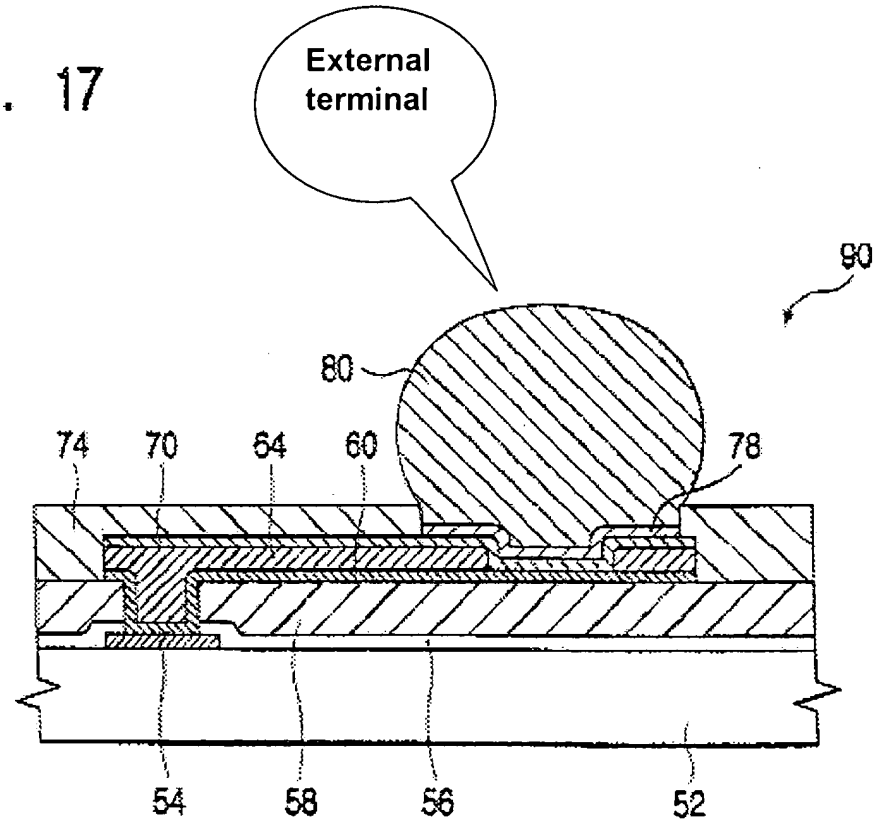

Concave portion
Inner surface of the through hole
Wiring layer
Polyimide/ Epoxy Resin layer
76
70
64
60
68
74
54
58
56
52

FIG. 17


External terminal
90
80
74
70
64
60
78
54
58
56
52

Regarding claims 4 and 12, Hwang discloses that an inner surface of the through hole in the resin layer 74 is in contact with the external terminal 80 (see Fig. 17 Labeled by the examiner above).

Regarding claims 5 and 13, Hwang (Fig. 17) further discloses a stress relaxation layer 58 (column 3, lines 66-67 through column 4, lines 1-2) disposed on the semiconductor chip 50, wherein the wiring layer 64 is disposed on the stress relaxation layer 58.

Regarding claims 6 and 14, Hwang discloses that the resin layer 74 is prepared from a solder resist of polyimide (column 5, lines 28-37).

8. Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hwang et al. (U.S. Pat. 6,455,408) in view of Hsuan et al. (U.S. Pat. 6,166,444) as applied to claim 1 above, and further in view of Farnworth et al. (U.S. Pat. 6,767,817).

Regarding claim 7, Hwang does not disclose that a circuit board comprising the semiconductor chip 90 disclosed in Fig. 17.

However, Farnworth (Fig. 2) teaches an integrated circuit package 36 (column 4, lines 1-3) including a circuit board 54 comprising a semiconductor chip 40 (column 4, lines 14-17). Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to provide a circuit board comprising the

semiconductor chip 90 of Hwang in order to form an integrated circuit package which is used in the desired electronic applications, as taught by Farnworth (column 4, lines 1-5).

Regarding claim 8, Hwang does not disclose that an electronic apparatus comprising the semiconductor chip 90 disclosed in Fig. 17.

However, Farnworth (Fig. 1) also teaches an electronic apparatus system 10 comprising an integrated circuit package 36 including a semiconductor chip 40 (Fig. 2 and column 4, lines 1-5). Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to provide an electronic apparatus comprising the semiconductor chip 90 of Hwang in order to form a desired electronic application such as a computer, audio or visual device, as taught by Farnworth (column 3, lines 15-21).

Double Patenting

9. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

10. Claims 1, 4-6, 7-9 and 12-14 are provisionally rejected under the judicially created doctrine of double patenting as being unpatentable over claims 12-27 of copending Application No. 10/801,093 (U.S. Pub. 2004/0245621). Although the conflicting claims are not identical, they are not patentably distinct from each other because both applications claim a semiconductor device comprising a semiconductor chip provided with an integrated circuit and a pad, and a wiring layer having a concave portion and electrically connected to the pad. Specifically, regarding claim 1 of instant application, claim 12 of copending application discloses a semiconductor device (claim 12, line 1), comprising:

a semiconductor chip provided with an integrated circuit and a pad that is electrically connected to the integrated circuit (claim 12, lines 2-3);

a wiring layer that has a concave portion and is electrically connected to the pad (claim 12, lines 4-5);

an external terminal that is joined to the concave portion of the wiring layer (claim 12, lines 10-11); and

a resin layer provided with a through hole and disposed on the wiring layer, the through hole and the concave portion residing at the same position (claim 12, lines 12-14).

Furthermore, claim 1 in the instant application is either broader version of claim 12 in the copending application or is obvious variations thereof. For example, claim 1 in the instant application claims "... the through hole and the concave portion residing at the same position" whereas claim 12 in the copending application claims "...the through hole and the concave portion overlapping each other". That shows no different meaning between these two elements. The facts are that the claims of the instant application and the copending application have claimed the same goal.

Regarding claim 9 of instant application, claim 21 of copending application discloses a semiconductor wafer (claim 21, line 1), comprising:

a semiconductor substrate provided with a plurality of integrated circuits and pads with each pad electrically connected to each of the integrated circuits (claim 21, lines 2-4);

a wiring layer that has a concave portion and is electrically connected to the pads (claim 21, lines 5-6);

an external terminal that is joined to the concave portion of the wiring layer (claim 21, lines 12-13); and

a resin layer provided with a through hole and disposed on the wiring layer, the through hole and the concave portion residing at the same position (claim 21, lines 14-16).

Regarding claims 4 and 12 of instant application, corresponding to claims 16 and 25 of copending application.

Regarding claims 5 and 13 of instant application, corresponding to claims 17 and 26 of copending application.

Regarding claims 6 and 14 of instant application, corresponding to claims 18 and 27 of copending application.

Regarding claims 7-8 of instant application, corresponding to claims 19-20 of copending application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Allowable Subject Matter

11. Claims 2-3 and 10-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record fails to disclose all the limitations recited in the dependent claims 2-3 and 10-11. Specifically, the prior art of record fails to disclose a width of the concave portion increases with a depth of the concave portion as recited in claims 2 and 10. The prior art of record also fails to disclose the concave portion has a first width at a first depth and a second width at a second depth that is deeper than the first depth, the first width being larger than an opening size of the concave portion and the second width being smaller than the first width as recited in claims 3 and 11.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Theresa T. Doan whose telephone number is (571) 272-1704. The examiner can normally be reached on Monday to Friday from 7:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, WAEL FAHMY can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you

have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Theresa Doan
September 27, 2005.